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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,393	11/17/2003	Hideyuki Noda	57454-990	2061
7590 06/24/2005				
McDermott, Will & Emery 600 13th Street, N.W. Washington, DC 20005-3096				
			EXAMINER TRAN, ANDREW Q	
			ART UNIT 2824	PAPER NUMBER
DATE MAILED: 06/24/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/714,393	<b>Applicant(s)</b> NODA ET AL.	
	<b>Examiner</b> Andrew Q. Tran	<b>Art Unit</b> 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 17 November 2003 and 09 March 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 18-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 18-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☒ Certified copies of the priority documents have been received in Application No. 09/632,333.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>11/17/2003</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Title*

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

--Semiconductor integrated circuit device having a logic circuit and a dynamic random access memory (DRAM) merged on the same chip--.

### *Double Patenting*

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 18-20 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1, 6 and 8 of prior U.S. Patent No. 6,649,984 to Noda et al. on November 18, 2003. This is a double patenting rejection.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sun et al. (US Pat. 5,920,779 hereafter "Sun"). See for example, Figs. 5A-5C and 6A-6C and corresponding descriptions thereof.

As to claim 18, Sun teaches a semiconductor integrated circuit device comprising a logic circuit (Fig. 6A) including a logic transistor (FET 50, 52, 54 or FET 56, 58, 60 with gate oxide layer approximately 40Å, see col. 8, ln. 22-30); and a memory circuitry (Figs. 6B and 6C) including a first circuit (Fig. 6B with gate oxide layer 44 of approximately 75Å, see col. 9, ln. 16-19) for receiving a first voltage (about 3.3v, see col. 8, ln. 62-64) and a second circuit (Fig. 6C) for receiving a second voltage greater than the first voltage (see col. 9, ln. 38-40, and also in Fig. 6C, the gate oxide of transfer FETs of embedded DRAM is approximately 100Å and thus inherently would withstand higher operating voltage than 3.3v). As to claim 19, see Fig. 6C. As to claim 20, the plurality of sense amplifier circuits could inherently be made in the substrate section B of Fig. 6B since various gate oxide thicknesses could be made depending on the type of MOS circuitry desired (see col. 7, ln. 38-44).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takebuchi (US Pat. 5,101,248 hereafter "Takebuchi").

Takebuchi teaches a semiconductor integrated circuit (IC) device comprising a logic circuit (Fig. 2C and rightmost part of Fig. 3C) including a logic transistor (Fig. 2C with an insulating film thickness B of about 250Å); and a memory circuitry (Fig. 2B and middle part of Fig. 3C) including a second circuit (Fig. 2B with an insulating film thickness C of about 450Å) for receiving a second voltage.

Takebuchi further teaches a high voltage transistor (Fig. 2A with an insulating film thickness C of about 450Å made in a leftmost part of Fig. 3C). And thus Takebuchi fails to teach a semiconductor IC device comprising a memory circuitry further including a first circuit for receiving a first voltage smaller than the second voltage.

However a permissible hindsight modification of the high voltage transistor of Fig. 2A in the leftmost part of Fig. 3C would be acceptable because Takebuchi readily recognizes the advantage of varying the thicknesses of the gate insulating film for improving operating speed (see col. 2, ln. 24 and col. 3, ln. 8-14). Further note that the thicker a gate insulating film is, the higher an operating voltage will become, as is well known in the semiconductor art.

Therefore it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the high voltage transistor of Fig. 2A with a transistor having a gate insulating film whose thickness D is smaller than thickness C of the memory transistor of Fig. 2B in order to improve operating speed, as taught by Takebuchi supra.

As to claim 19, see Fig. 2B. As to claim 20, it would have been obvious to make a plurality of sense amplifier circuits with transistors having a gate insulating film with thickness D as set forth above.

**Conclusion**

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Liu et al. (US Pat. 6,420,248) describes a double gate oxide layer method of manufacture.

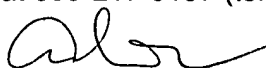
Yamada et al. (US Pat. 6,445,047) describes a semiconductor device and method for fabricating the same.

Takebuchi (EP Pub. 0 443 603) describes a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Q. Tran whose telephone number is (571) 272-1885. The examiner can normally be reached on Mon - Fri 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Andrew Q. Tran

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Primary Examiner  
Art Unit 2824

at  
June 21, 2005